WHITE PAPER

Modular embedded technologies for cognitive RF and EW systems

abaco SYSTEMS

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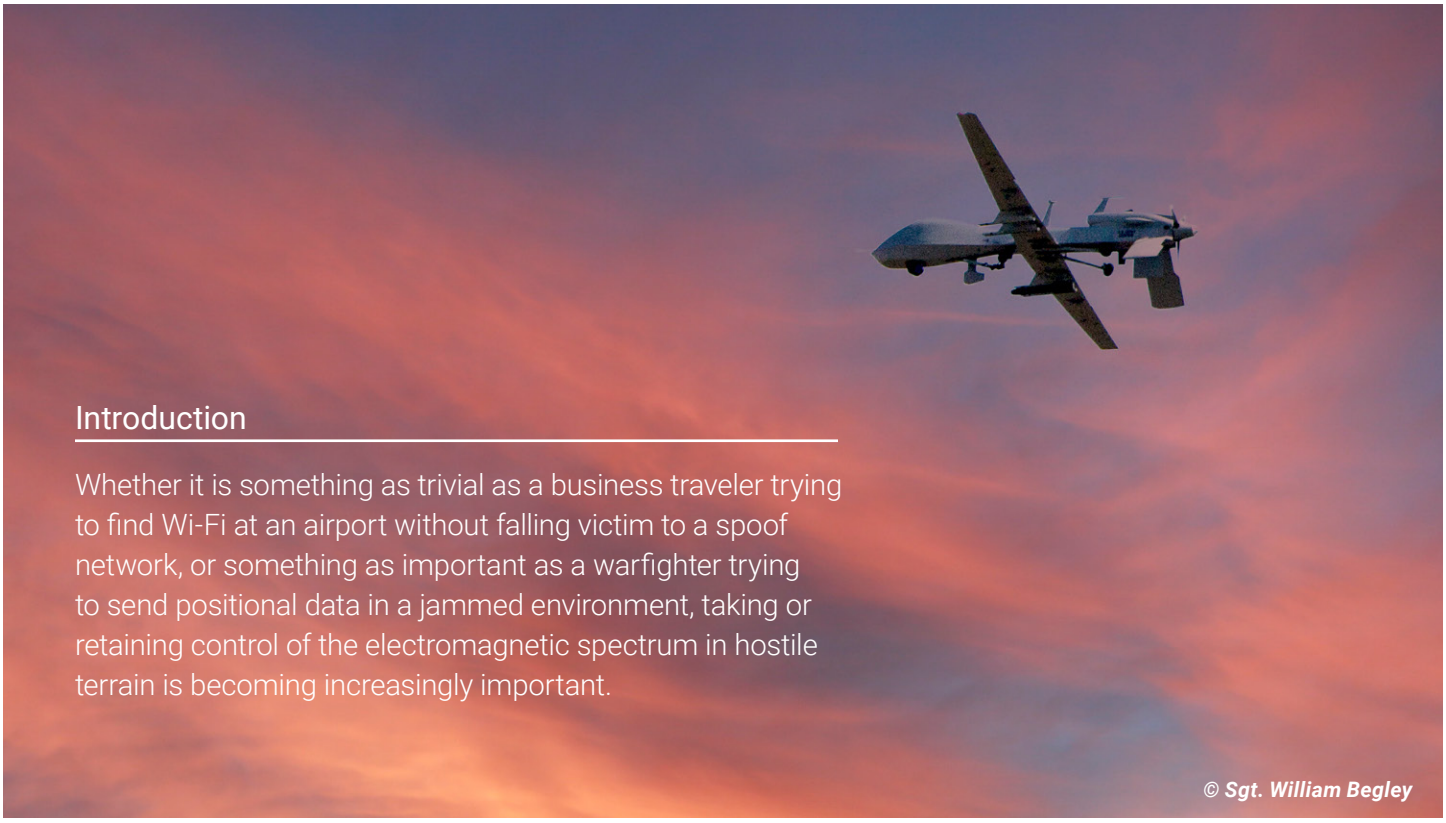

Introduction

Whether it is something as trivial as a business traveler trying to find Wi-Fi at an airport without falling victim to a spoof network, or something as important as a warfighter trying to send positional data in a jammed environment, taking or retaining control of the electromagnetic spectrum in hostile terrain is becoming increasingly important.

For many business travelers, their phone includes a number of techniques to improve signal quality based on the spectrum available - but travelers also develop their own set of heuristics based on previous experience. Some of these are environmental (there's a café; there will probably be good Wi-Fi signal there); some are based on experience (don't connect to a hotspot called "Jim's big phone"); and some need to be developed on the fly (this looks like a hotel hotspot but the login page seems odd, I'm not going to use it just in case).

What these travelers are essentially doing is a process of sense, learn, and adapt – something that's at the heart of current research into cognitive RF and cognitive EW.

The need for speed

The increased movement in radar and EW systems away from fixed analog systems towards fully digitally programmable systems has allowed both to increase their operational frequency ranges, using frequency agility and/or advanced modulation techniques. For radar systems, these techniques mean that they are harder to detect but also harder to jam or spoof. This results in radar systems that are harder to jam or spoof.

These new methodologies, often described as cognitive RF and cognitive EW, rely on reconfigurable hardware and software that can detect, learn about, and adapt to new threats in the field during a mission.

As radars leverage wider bandwidths, including frequency agile 'hopping' signals and Low Probability of Intercept (LPI) techniques, jamming and interference technologies also need to increase their operational frequency ranges. The net result is a processing power and bandwidth escalation race–one that is becoming increasingly fast paced.

Traditionally, radar and EW systems deployed countermeasures developed in response to a static threat library. In this operational mode, the system was designed and thoroughly tested to counter known threats.

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If an unknown threat was detected, some generic countermeasures may have been employed, but, in general, information was gathered on the new threat for post-mission analysis. Further analysis was then conducted in a laboratory and an update to the static threat library was tested and issued. The process could take months, or even years. This methodology was fine when the upgrade process for the threats followed a similar timetable.

Need for Flexibility and Adaptability

Another emerging issue is the fielding of these new countermeasures. Older systems may be difficult to upgrade, requiring the removal and replacement of memory on the system. Modern systems have evolved to the point that the threat library can be updated on the operational battlefield by plugging a secure computer into a port on the platform. Future capabilities envisage the ability to update these threat libraries literally on the fly.

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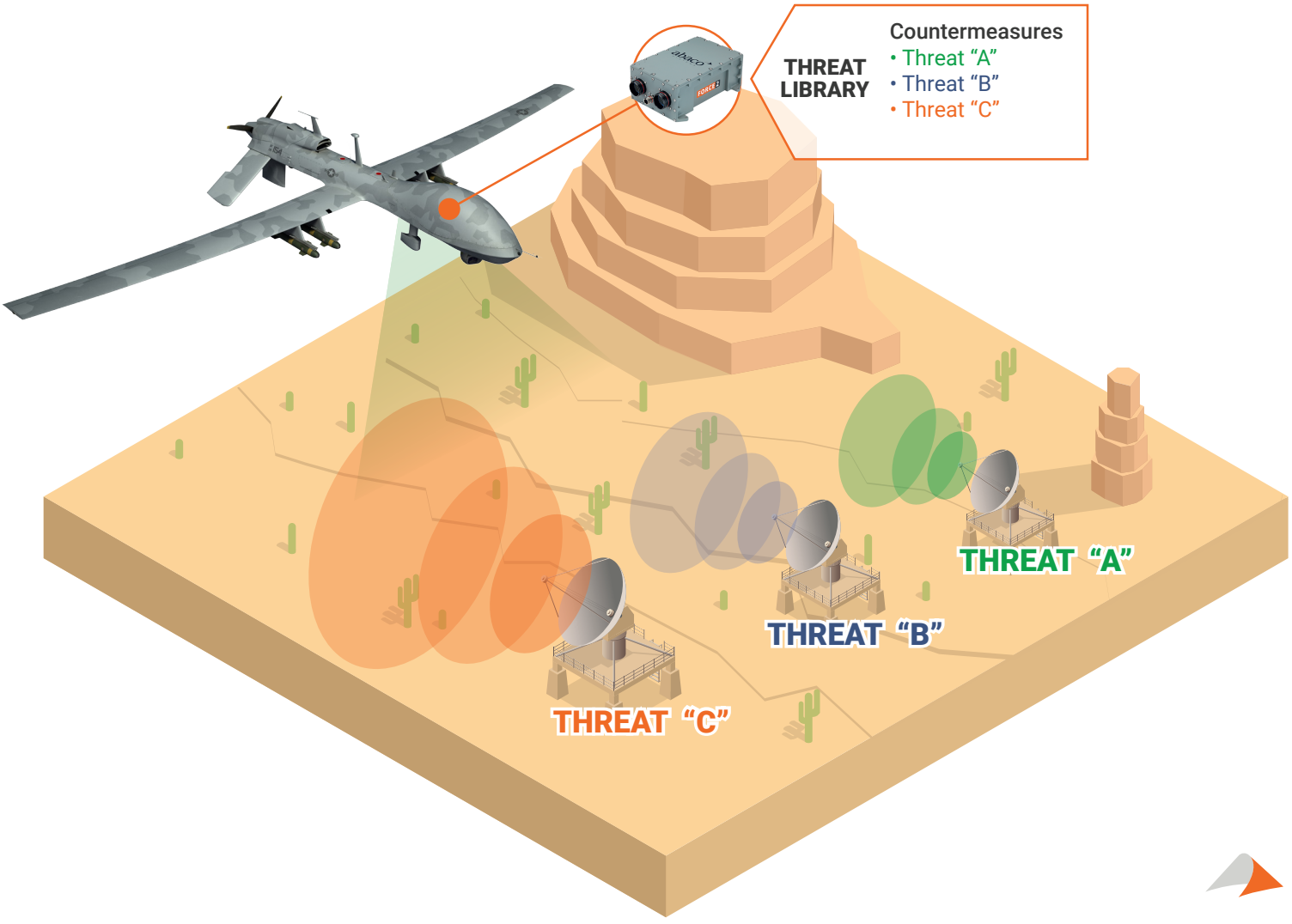
To enable this, the learn-and-adapt process for the threat library becomes a feedback loop, enabling new countermeasures to be developed on the fly. This requires a significant processing performance leap, one that must be accomplished without a significant increase in size, weight, and power.

This new methodology is referred to as cognitive and machine learning EW systems at the tactical edge.

Static Intelligence Threat Library



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Reconfigurable hardware

Cognition in EW systems is needed because it is envisaged that during a real-world conflict, traditionally-static threats, such as an adversaries missile fire control RADAR, will switch into new, unknown modes that have not been encountered before and consequentially have no countermeasure in the threat library. In other words, new EW systems need to be able to detect and counter unknown threats. This requires a large amount of computing resources, and a heterogeneous system uses three main compute elements to address the required resources - FPGA, GPGPU and host-based CPU. Each compute element provides a complimentary capability.

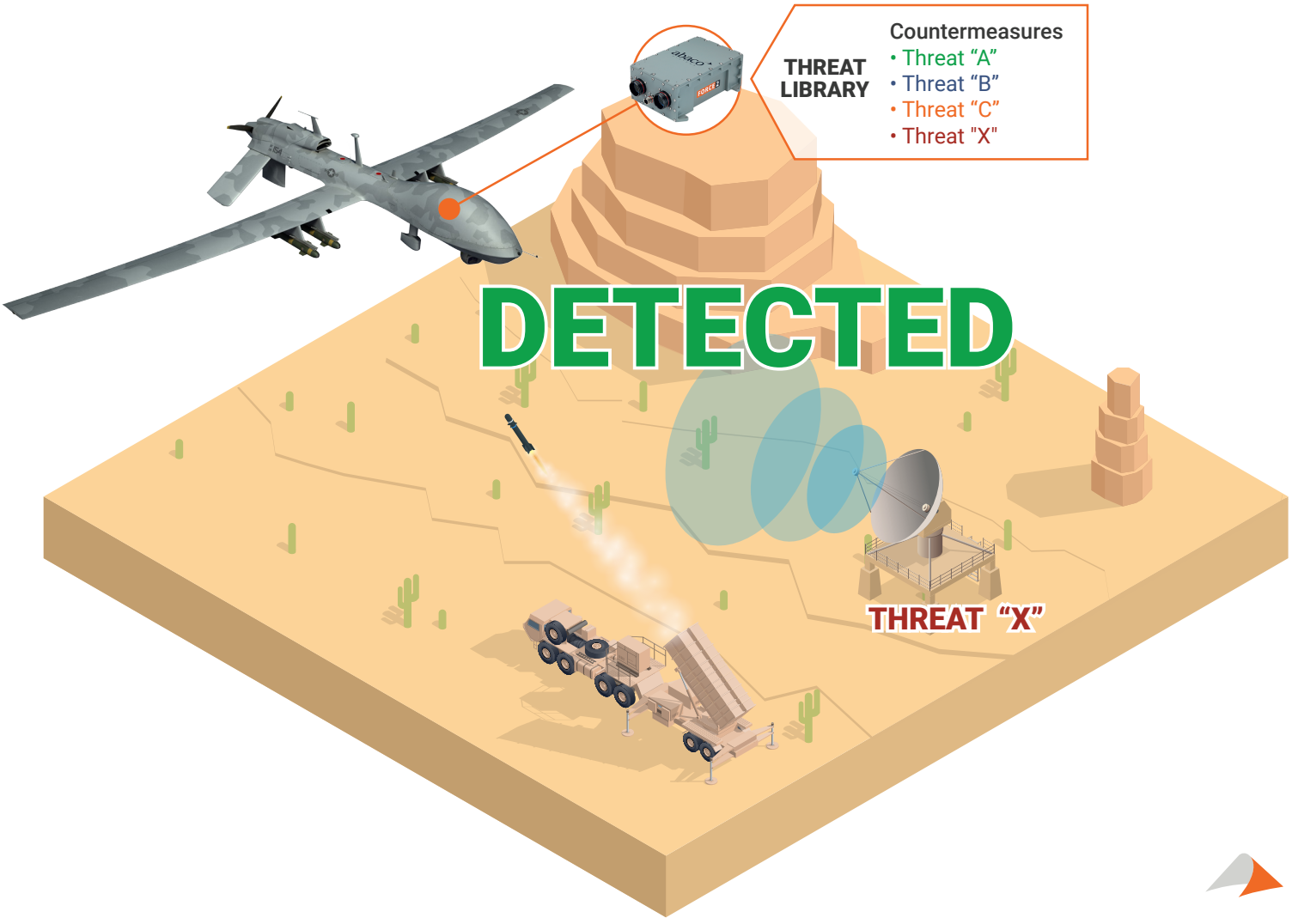
FPGAs excel at high-bandwidth, low-latency front-end RF processing tasks such as energy detection and digital down conversion, for example.

FPGAs are also ideal at processing very high data rates associated with wideband receivers and in processing many such streams of data to perform digital beamforming or nulling. Modern modular architectures also provide backplane data transports and switches to move huge amounts of data in real time between these compute elements at speeds over 100Gb/s. FGPAs also excel at fixed point processing.

A GPGPU, on the other hand, provides vast amounts of parallel-processing floating-point compute elements that provide a flexible space for complex artificial intelligence (AI) and machine learning (ML) algorithms that can be developed in traditional programming languages such as OpenCL, CUDA and Halide.

Finally, high performance multi-core CPUs allow both continued refinement of the processed data in a rich floating-point environment using languages such as C# and Python as well as providing communications, system security, operator interface and data storage.

Static Intelligence Threat Library



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Challenges remain in system implementation, such as disparate tool chains for the compute elements and the need to standardize software module-level interfaces. A recent development that promises to ease the task of moving data between compute elements is the Photon initiative. Photon was developed by The MITRE Corporation and is a framework that enables efficient delivery of digital signal information to both CPU and GPGPU based signal processors and was adopted by the US Army to ensure consistency across the development of all EW-based solutions.

Photon is an enabler for implementing modular and re-usable AI/ML capabilities at a tactical level and unifies multiple stovepipe processing frameworks and detectors onto a single platform. Photon provides a modern foundation for converging SIGINT, EW, and Cyber capabilities.

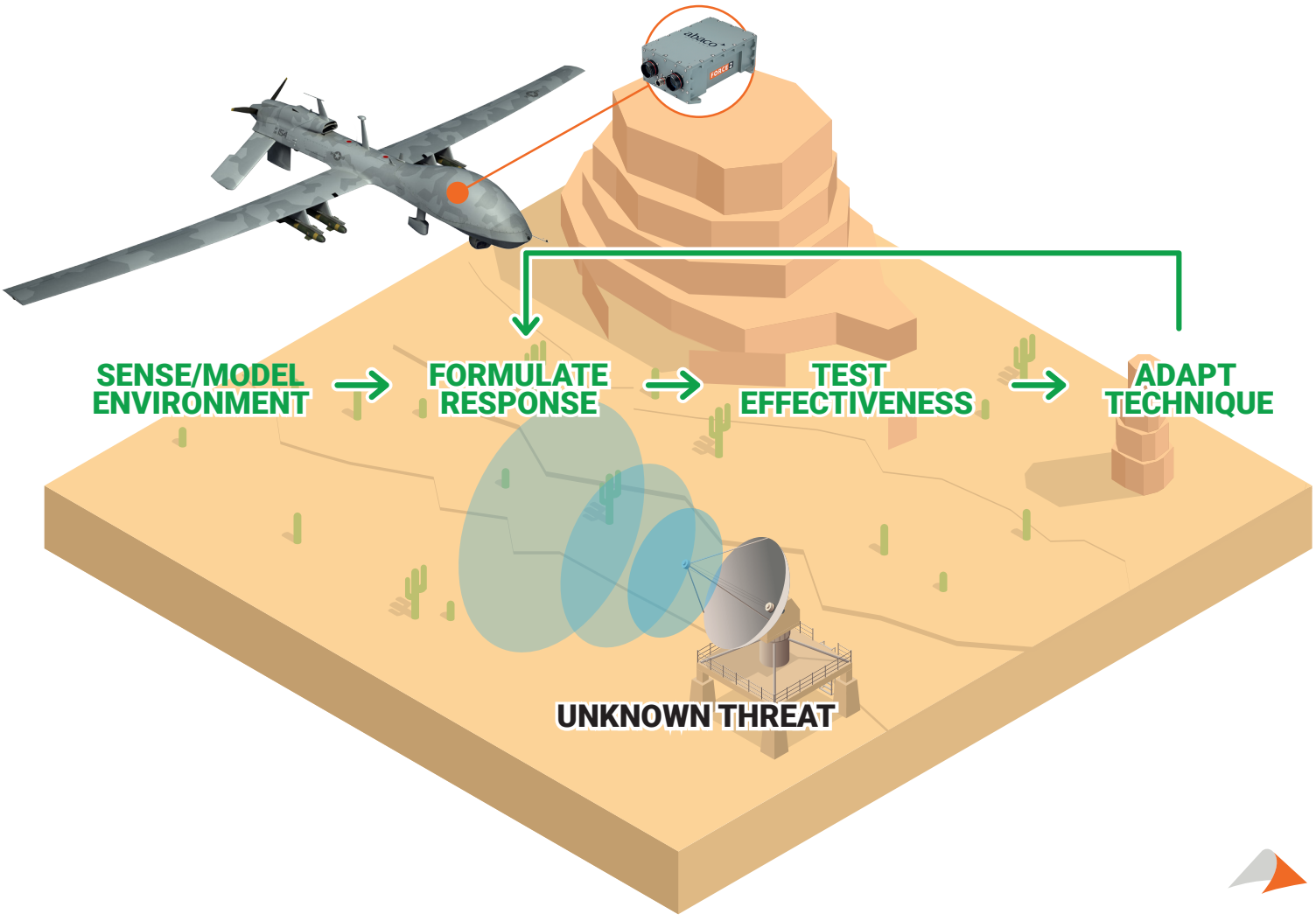
Optical extensions of the VPX backplane such as VITA 66.4 provide additional protocol-agnostic high-speed optical lanes for extra inter-board communication. 3U VPX provides high processing power per watt, per cubic inch, and per ounce, and solutions can be tailored to every environment. In addition, the use of standards based interfaces such as OpenVPX (VITA 65), VPX (VITA 46.0), FMC (VITA 57.1), and FMC+ (VITA 57.4) simplify future hardware upgrades.

Wanted: low latency processing powerhouse

As we've seen, cognitive systems require multiple channels and wide RF bandwidths – meaning the data throughput that needs to be processed is massive. However, processing architecture is just one of the technology challenges that need to be overcome for modern RF and EW systems.

In this section, we consider end-to-end system latency, as data needs to be moved and processed as quickly as possible with minimal buffering or lag between input and output.

Static Intelligence Threat Library



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This kind of system is conventionally referred to as a Digital RF Memory (DRFM). A DRFM system is a low-latency closed loop threat/response system designed to counter RF threats within a time window that ensures the originator does not detect the DRFM effect. The most common applications for a DRFM are jamming and spoofing of RADAR signals, which can be used to deceive the receiver as to the natural signature of the target, or to create false targets, for example. A key feature of the DRFM is coherence, meaning it is coherent with the source transmission, which implies a very low latency from RF input (detection) to RF output (effect).

The FPGA is a key technology enabler for cognitive systems because of its ability to handle constant streams of high-speed data with low latency. As cognitive radar and EW techniques continue to develop, the demand for significant front-end processing resources dramatically increases.

Since cognitive systems often leverage adaptive beamforming and phased arrays, the heavy lifting of signal processing has been moving further and further toward the front-end. Because of its superior ability to undertake stream-based processing using highly-parallel operations, inserting a high-performance FPGA to perform data acquisition and initial signal processing can significantly enhance performance while reducing power consumption and latency. This leaves the less deterministic tasks to either the CPU or GPU on the back end of the system.

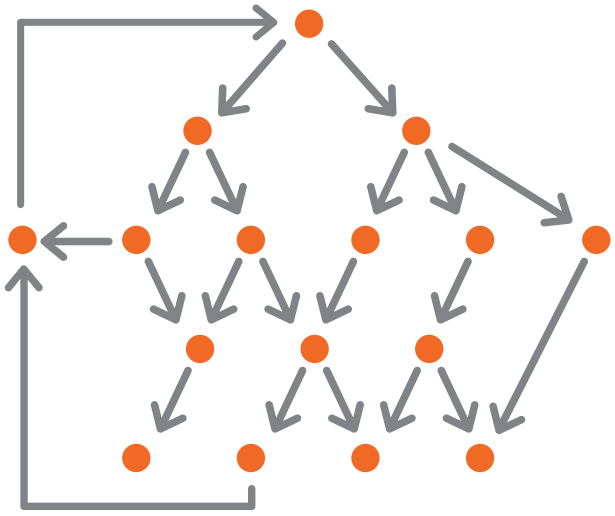
Revolutionary technology

As we established earlier, a bandwidth escalation race is a key component of RF and EW system development, and analog RF performance is key. To overcome this challenge, Abaco Systems offers two different approaches to digitizing the necessary data and getting it into the FPGA as quickly as possible.

In many cases, we utilize our industry-leading FMC and FMC+ (VITA 57.1 and VITA 57.4) portfolio of high performance analog-to-digital conversion modules. FMC+ allows the use of modular ADC/DAC boards that employ a low-latency interface directly into the high-speed transceiver of a modern 3U VPX FPGA carrier such as the VP889, which features a Virtex UltraScale+ FPGA, Zynq Ultrascale+ MPSoC, and an FMC+ site. The use of a mezzanine standard such as FMC+ also enables the ADC card to be easily upgraded so that modern high-speed ADC technology from companies like Texas Instruments can allow direct RF sampling.

Cognitive EW Computing Requirements

Streaming Computation
Field Programmable Gate Array (FPGA) Polarity



Complex Branching Decision Tree
General Purpose Processor (GPP)
Deep Learning Algorithms
Graphics Processors (GPU)

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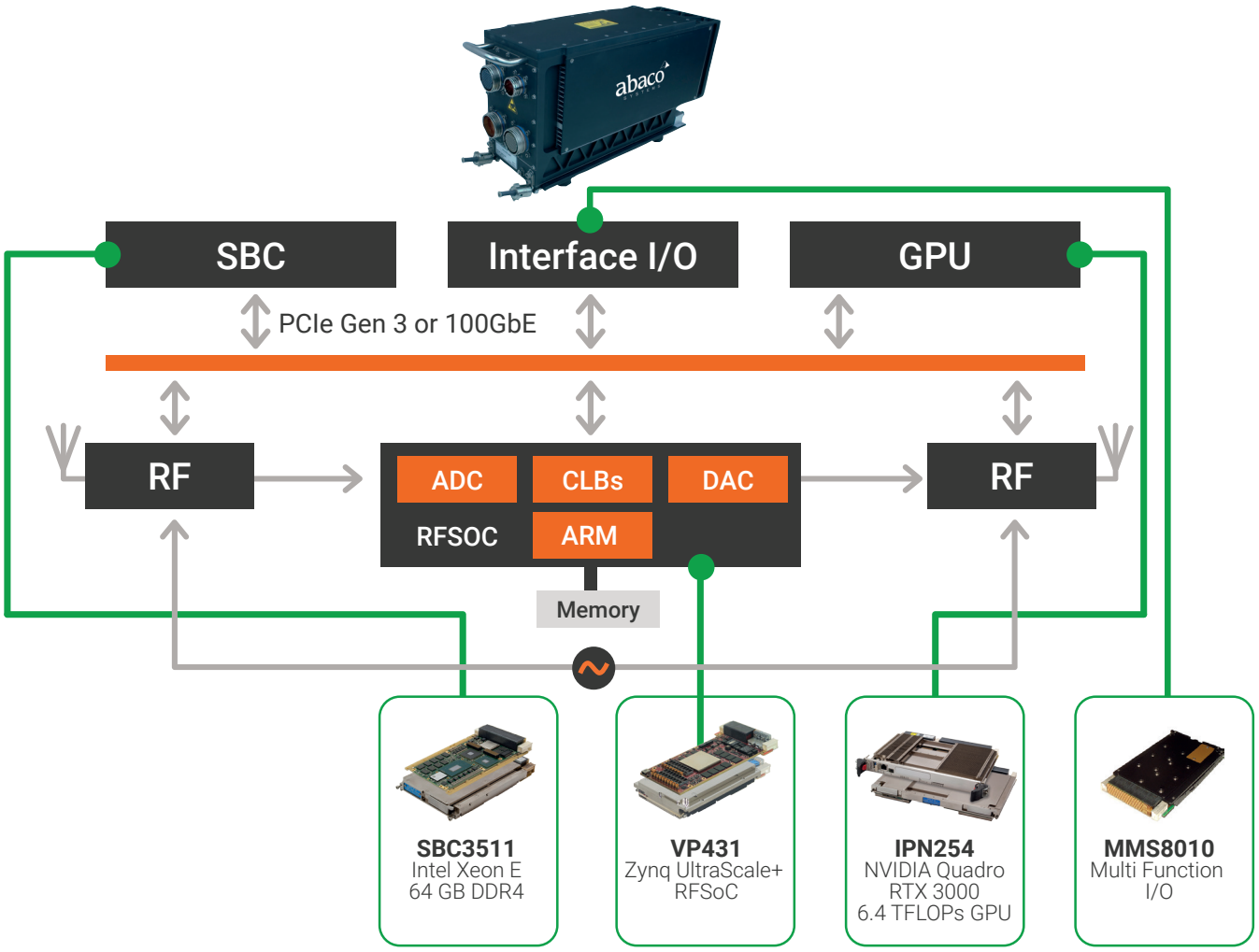
The second and newer approach is to leverage the revolutionary RF System-on-Chip (RFSoC) technology from Xilinx®, the first FPGA processor to integrate multi giga-sample ADCs and DACs into a SoC architecture. The Zynq® UltraScale+™ RFSoC features an integrated ADC, DAC, configurable logic elements, multi-processor embedded Arm® Cortex-A53® application processing unit (APU), and an ARM real time processing unit (RPU). This enables input/output channel density to be maximized while reducing the RF signal chain complexity. The benefit is a reduction in system latency and an ideal balance between channel density and signal processing capabilities.

As an example, the Abaco VP431 3U VPX RFSoC board features an integrated 8-channel, 14-bit ADC sampling at 4.0 to 5.0 GSPS and an integrated 8-channel, 14-bit DAC sampling at 6.4 to 10 GSPS. This simplification reduces system latency and enables users to leverage the programmable logic in the FPGA for other tasks that are essential to cognitive countermeasures.

Additionally, the heterogeneous processing capability of the VP431 enables the utilization of the embedded ARM Cortex processor for decision and control processes – optimizing the efficiency of the GPGPU or CPU, or in some applications, eliminating the need for an additional processor entirely.

When additional processing is required, the system developer will face challenges in how to handle the extreme volume of data produced when the system includes multiple channels with high data rates.

COTS Electronic Warfare System



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Many times, a system is limited by the data connection fabric. The VP431 has a traditional VPX data plane interface, allowing a x4 PCIe Gen3 connection to a host computer. With eight ADCs sampling at rates over 5GSPS with two bytes per sample, even a modern PCIe Gen 3 high speed data connection cannot accommodate data transfers at this speed.

To overcome this challenge, the VP431 includes – in addition to the PCIe® Gen3 data plane - the option for an 8-channel VITA 66.4 fiber optic link, permitting 2 x 100Gb/s links . Previous technologies would have taken four times as many boards to achieve the same level of performance and integration.

The increasing role of Unmanned Aerial Systems (UAS) in EW

UAS are the ideal platform for both stand-in and stand-off jamming and Intelligence Surveillance and Reconnaissance (ISR) missions. The UAS can carry a larger payload when compared to a similarly sized manned platform. However, and more importantly, it enables execution of dangerous and/or difficult tasks safely and efficiently at lower operating costs without putting aircrew in potentially deadly situations.

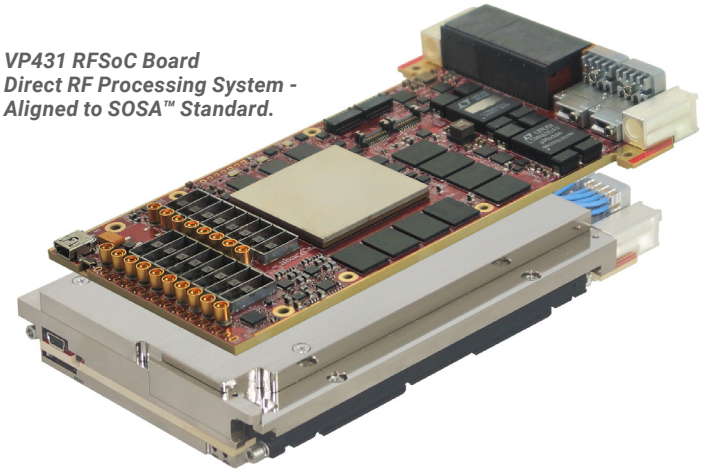
A challenge of many UAS is reducing the size, weight and power (SWaP) of the EW system due to the reduced payload of many smaller UAS. This is a driving influence behind the use of cost-effective industry standards like the Sensor Open Systems Architecture (SOSA™) standard. A 3U VPX system aligned to the SOSA standard can address the SWaP challenges in a high-bandwidth heterogeneous computing environment.

An example of an evolving UAV EW program is the US Army's Multi-Function Electronic Warfare – Air Large (MFEW-AL). MFEW-AL uses an airborne EW pod mounted aboard an MQ-1C Gray Eagle UAS. The Gray Eagle is the latest version of the venerable General Atomics MQ-1B Predator UAS. MFEW-AL provides brigade commanders two new capabilities. The first is an organic electronic attack and jamming capability and the second is electronic support, which provides electromagnetic sensing and collection capabilities. MFEW-AL includes requirements to conduct offensive electromagnetic cyberattacks.

Conclusion

Cognitive processing and the constant need for more bandwidth is significantly driving up the performance requirements of radar and EW processing subsystems, while the availability of size, weight, and power is being driven down.

These requirements can be successfully addressed through the use of advanced technologies such as multi-core processors, GPUs, and Xilinx's RFSoC and Zynq MPSoC FPGA, allowing developers to focus on radar prototyping of suitable cognitive and digital processing algorithms. For next generation cognitive radar and EW systems, the VP431 and similar products can provide the necessary edge over adversaries in end-to-end latency and system performance.



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